Transparent Flexible Organic Transistors Based on Monolayer Graphene Electrodes on Plastic

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There has been much interest in graphene-based electronic devices because graphene provides excellent electrical, optical, and mechanical properties.[1] In this sense, organic electronic devices using graphene electrodes have attracted considerable attention, and several reports have described the use of graphene source/drain electrodes in organic field-effect transistors (OFETs).[2] One of the ultimate goals in the fabrication of OFETs using graphene electrodes lies in the fabrication of flexible and transparent organic transistors, assembled on plastics substrates, that maintain their high performance under ambient conditions. However, no reports have described the fabrication of organic transistors assembled on plastic substrates because the synthesis of either graphene or reduced graphene oxide requires high-temperature fabrication processes.

Another important goal in the context of fabricating organic electronic devices with graphene electrodes lies in the fabrication of highly transparent graphene electrodes that cover large areas. Graphene transmittance decreases linearly as the number of layers increases in n-layer graphene.[3] Thus, the use of monolayer graphene is necessary to achieve high transparency in graphene electrodes, provided that the conductivity of the graphene is sufficient for device electrode applications. Another merit of monolayer graphene is its extremely low thickness (3–4 Å). Source/drain electrodes in staggered bottom-contact FET structures should be thin to ensure step coverage of the active layer during sequential transistor fabrication.[4] For this reason, one-atom-thick monolayer graphene provides ideal source/drain electrodes for efficient charge injection. Recently, several groups succeeded in fabricating high-quality/large-area graphene with preferential monolayer thickness using a chemical vapor deposition (CVD) method.[5,6] Thus, it may be possible to utilize monolayer graphene electrodes in flexible transparent OFETs with monolayer graphene source/drain electrodes.

Here, we have developed high-performance bottom-contact pentacene FETs with graphene source/drain electrodes by transferring and patterning CVD-grown monolayer graphene films in a room-temperature process. The advantages of the transferred graphene electrodes relative to common metal electrodes are discussed. Furthermore, carbon-based organic transistors using graphene electrodes were assembled on plastic substrates, and they showed excellent electrical properties with both flexibility and transparency.

Graphene was synthesized on a copper foil following the CVD process (see Experimental Section for details).[5] Because CVD was conducted in a quartz tube with heating to 1000 °C, appropriate transfer procedures were followed to successfully apply the graphene for fabrication of electronic devices. Here, we used a polymer-supported transfer method on an arbitrary substrate to use graphene as a transparent/conductive electrode for organic transistors.[7] **Figure 1**a shows a schematic of the fabrication steps for patterning source/drain electrodes using a polymer-supported transfer method. The UV absorption spectrum showed that the graphene electrode was highly transparent, with a transmittance of 97.6%, and Raman spectroscopy revealed that the graphene film was high in quality and preferentially formed monolayers (Supporting Information (SI), Figure S1). The sheet resistance of the graphene film was measured to be ≈0.5 kΩ sq^{-1} using the four-point probe method. The merits of graphene electrodes are not confined to their high conductivity and transparency. Because graphene consists only of a planar honeycomb lattice that is one carbon atom in thickness, the film may easily be patterned by conventional photolithographic techniques combined with reactive ion etching (RIE). Furthermore, sheet resistance of patterned graphene electrode maintains the original value of ≈0.5 kΩ sq^{-1}, confirming the utility of the suggested patterning process. Figure 1b shows patterned monolayer graphene source/drain electrodes on a SiO_2/Si substrate, exhibiting a clear patterned image of the graphene films.

The feasibility of using monolayer graphene as source/drain electrodes in OFETs was demonstrated by depositing pentacene on a SiO_2/Si substrate that had been patterned with graphene electrodes. Because the growth characteristics of pentacene films on source/drain electrodes are important for optimizing the electrical properties of pentacene FETs,[8] atomic force microscopy (AFM) images of graphene and pentacene films were obtained and are shown in Figure 1c. The graphene surfaces presented many small areas of residue that may have

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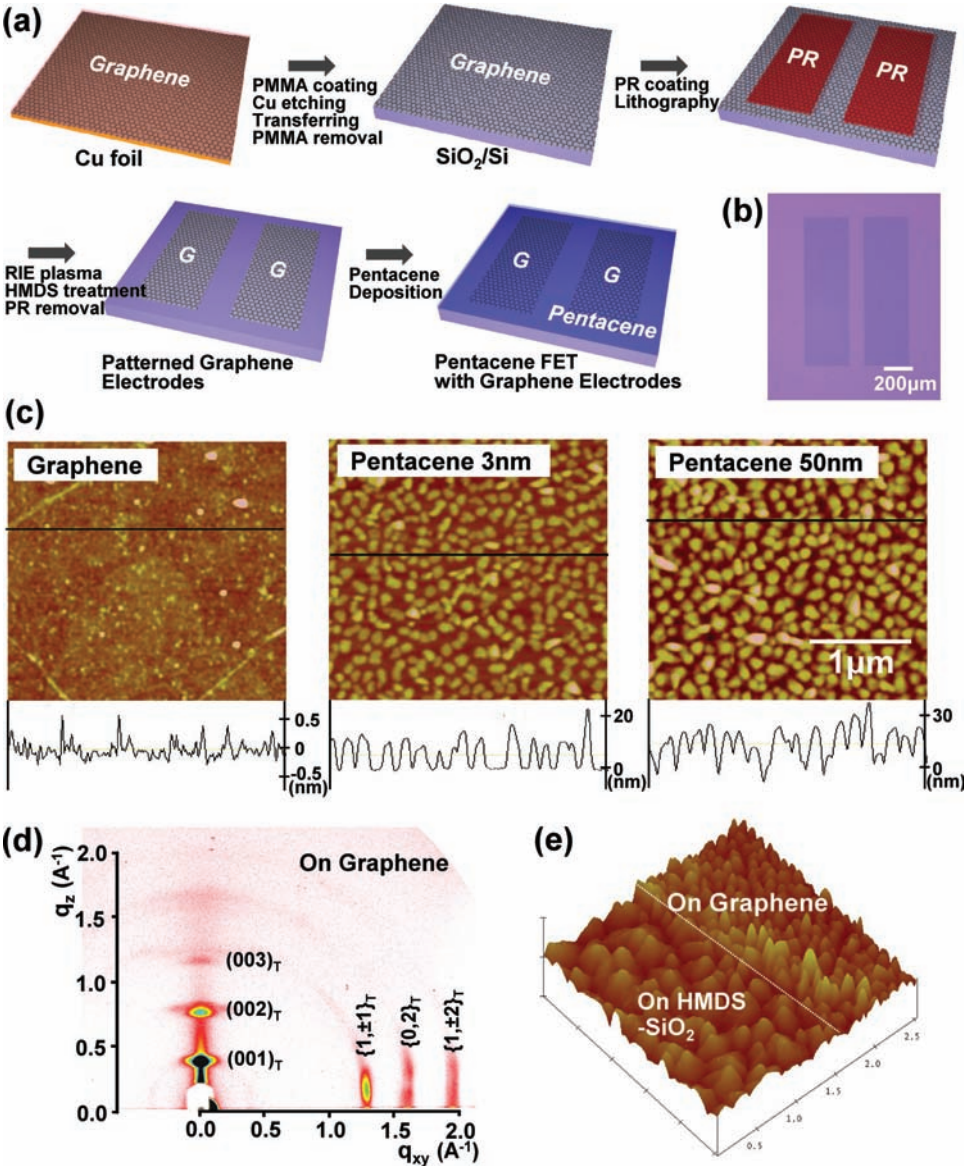

Figure 1. a) Schematic of the fabrication of pentacene FETs with monolayer graphene electrodes on a SiO_2/Si substrate. b) Optical microscopy image of patterned graphene electrodes. c) AFM images of graphene films after photolithography and 3 nm, 50 nm-thick pentacene films on graphene films. d) 2D-GIXD pattern for pentacene films (10 nm) on graphene films. e) AFM images (2.5 μm × 2.5 μm) of the pentacene films (50 nm) at the boundary between the hexamethyldisiloxane (HMDS)-treated SiO_2 surface and a graphene electrode. PMMA = polymethylmethacrylate; PR = photoresist.

originated from the PMMA and photoresist (see AFM line scans in SI, Figure S2).[9] These residues remained on the surface of the graphene during our polymer-supported transfer method, although other methods using metal/polymer bilayer supports were known to reduce these residues.[10] Pentacene deposited on graphene electrodes with residues underwent 3D growth, as shown in the 3 nm, 50 nm-thick pentacene AFM images. This growth mode is commonly observed on dielectric substrates with a low surface energy, on which molecule–substrate interactions are relatively weak.[11]

Figure 1d shows 2D grazing incidence X-ray diffraction (2D-GIXD) patterns of 10 nm-thick pentacene films deposited on a graphene electrode. Intense (00l) crystal reflections along the q_z direction suggest that most pentacene molecules were oriented with their long axes directed toward the surface normal (vertically aligned). Furthermore, three intense in-plane reflections, {1, ±1}, {0, 2}, {1, ±2} in the thin film phase reflections, appearing vertically oriented at a given q_{xy}, suggest that the pentacene molecules were arranged in a herringbone packing structure that consisted of multilayered structures. This arrangement and packing geometry for pentacene molecules are common to dielectric substrates, including self-assembled monolayer-modified SiO_2 substrates.[12] It should be noted that pentacene molecules on highly oriented pyrolytic graphite (HOPG) surfaces adopt a lying-down orientation.[13] Because the surface properties of graphite are the same as those of graphene, pentacene

molecules on a clean graphene surface are also assumed to adopt this orientation. However, the surface properties of the patterned graphene electrodes differed totally from those on clean graphene surfaces because the polymer residues were inevitably physisorbed on the graphene surface, as shown in Figure 1c. This result suggests that the growth characteristics of pentacene on patterned graphene electrodes are determined by the residue that covers the graphene surface, rather than the π–π interactions with graphene.

In the bottom-contact device configuration, the morphology of the organic semiconductors at the interface between a channel and electrode is central to efficient charge transport from the electrode to the channel. Figure 1e shows AFM images of pentacene films at the interface between an HMDS-treated SiO_2 and a graphene electrode. Although the grain size of the pentacene domains on the graphene electrode was smaller than that of the pentacene domains on the channel region, pentacene grains grew continuously at the interface between the channel and the electrode, and no discernable transition regime was observed between them. Continuous grain growth may originate from the orientational homogeneity of pentacene in the channel and electrode regions, as revealed by a structural analysis of pentacene films on the patterned graphene electrodes. Notably, the growth of pentacene grains was not limited by the thickness of the electrode, because patterned monolayer graphene electrodes were significantly thinner compared to common metal electrodes. Thus, efficient charge transport from the graphene to the channel is guaranteed, provided that injection barrier from the graphene to the channel is sufficiently low.

The electrical properties of pentacene FETs with monolayer graphene electrodes were characterized by measuring the output and transfer characteristics of these devices, as shown in **Figure 2**a,b. The output curve shows the desirable linear and saturation regimes with a clear gate–voltage dependence. The transfer curve showed a low off-current level of $\approx 10^{-11}$ A and a high current on/off ratio exceeding 10^7. The field-effect mobility was calculated from measurements taken from 15–20 devices in the saturation regime. The bottom-contact pentacene FETs based on graphene source/drain electrodes had an average field-effect mobility of 0.54 ± 0.04 $cm^2\ V^{-1}\ s^{-1}$ (maximum field-effect mobility of up to 0.6 $cm^2\ V^{-1}\ s^{-1}$). For comparison, thermally-evaporated Au electrodes were used as source/drain contacts for bottom-contact pentacene FETs, holding the other device fabrication steps constant. The field-effect mobility of FETs using Au electrodes was 0.02 $cm^2\ V^{-1}\ s^{-1}$ (SI, Figure S3), which was much lower than the mobilities of FETs fabricated with graphene electrodes.

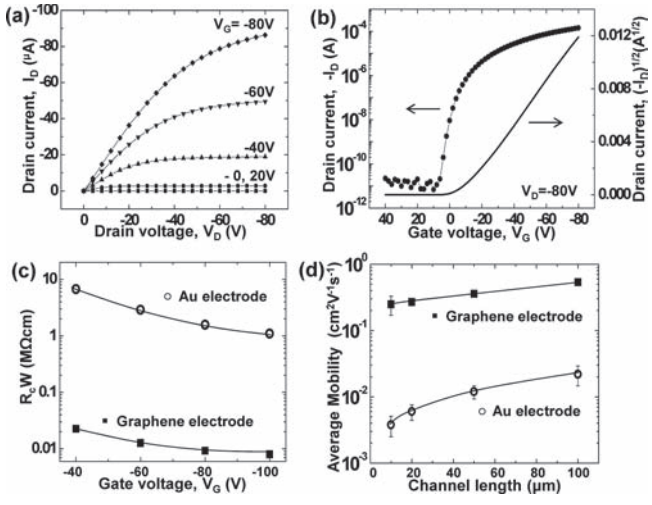

Figure 2. Electrical properties of pentacene FETs with monolayer graphene electrodes on a SiO_2/Si substrate. a) Output characteristics, b) transfer characteristics of FETs with graphene electrodes (L = 100 μm, W = 1000 μm). c) Calculation of the contact resistance values. d) Channel length-dependent field-effect mobilities. Electrical properties of FETs with Au electrodes are shown for comparison.

To assess the influence of the electrode material on the electrical contact between source/drain electrodes and the pentacene films, the contact resistances of graphene and Au electrodes were calculated using the transfer line method (SI, Figure S4).[14] The contact resistance of the graphene electrode, normalized by the channel width, decreased from 0.02 to 0.008 MΩcm as V_G varied from –40 to –100 V (Figure 2c). In contrast, the contact resistance of the Au electrode at a given V_G exceeded that of the graphene electrode by more than two orders of magnitude. Therefore, charge injection and transport were much more efficient in the graphene electrode than in the common metal electrode (see SI, Figure S5,6,7 and text). Because the contact resistance dominates the total resistance in devices with a short channel length, the field-effect mobility was found to decrease as the channel length decreased. However, the magnitude of this decrease in field-effect mobility was much higher for devices with Au electrodes because the contribution of the contact resistance at the Au electrode was much more significant than that at the graphene electrode (Figure 2d). The contact resistances of graphene electrodes are more or less similar to those of single-walled carbon nanotube (SWCNT) composite electrodes.[15] Although the sheet resistance of monolayer graphene ($\approx$0.5 kΩ sq^{-1}) is higher than that of SWCNTs ($\approx$0.27 kΩ sq^{-1}),[16] graphene is significantly thinner than SWCNTs, and thus the patterning process of graphene is much more convenient.

Because steps for fabricating graphene electrodes are compatible with plastic substrate processing, pentacene FETs were assembled on flexible plastic substrates following transfer and patterning of the graphene electrodes (T–P process), as shown in Figure 1a. Instead of using a SiO_2/Si substrate, polyarylate, poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonic acid (PEDOT/PSS), and crosslinked poly-4-vinylphenol (PVP) were used as the plastic substrate, gate-electrode, and gate-dielectric, respectively. The field-effect mobility of the resulting device fabricated by the T–P process was relatively low ($\approx$0.01 $cm^2\ V^{-1}\ s^{-1}$, see **Figure 3**c). To investigate the cause of this undesirable behavior, the surface morphologies of PVP and pentacene films grown on PVP were characterized by AFM, as shown in Figure 3d. The surface of PVP had a high RMS roughness of 2.9 nm, and thus the grain size of the pentacene film grown on the PVP surface was relatively small ($\approx$100 nm). We surmised that RIE, applied to remove the graphene film that was not covered by the photoresist, damaged the underlying PVP, resulting in a rough and hydrophilic PVP surface.

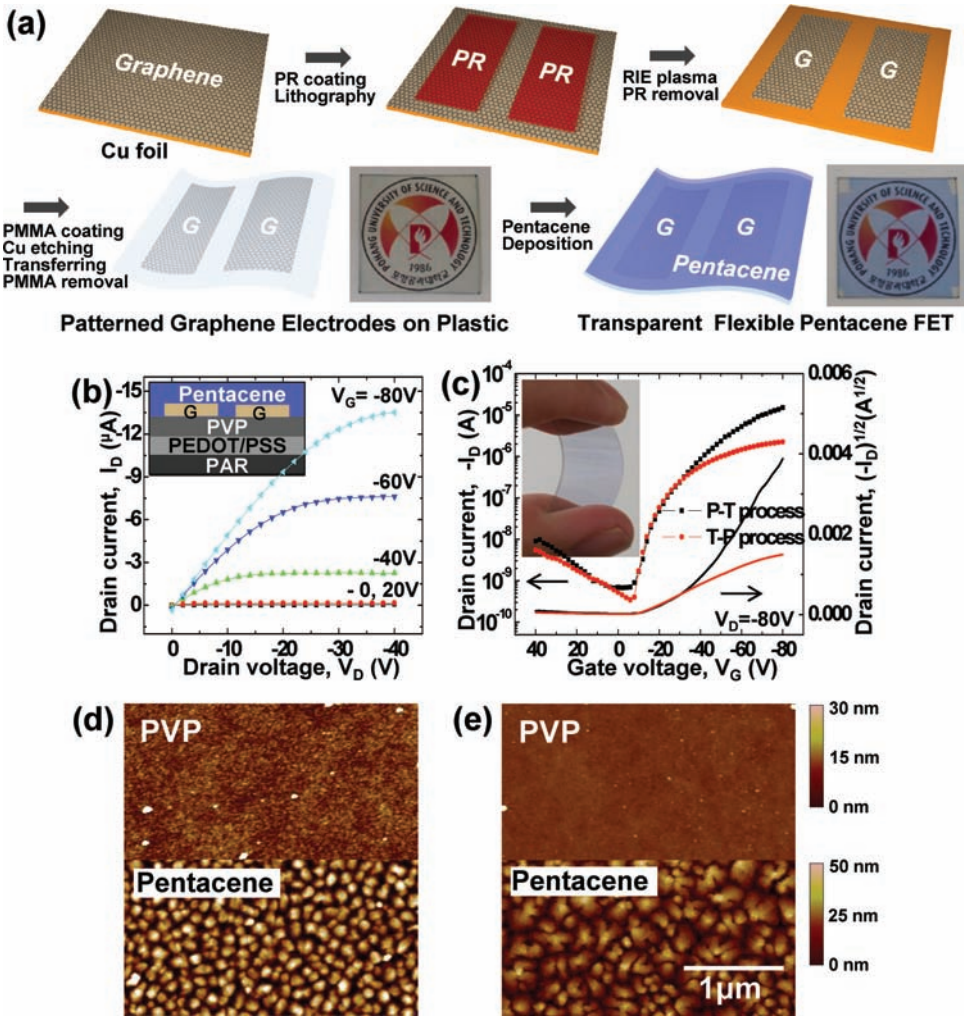

Figure 3. Characteristics of transparent flexible pentacene FETs with monolayer graphene electrodes on a plastic substrate. a) Schematic of the procedure for fabricating patterned graphene electrodes on a plastic substrate. Digital camera images of flexible/transparent FETs with graphene source/drain electrodes before and after pentacene deposition are also shown. 120 FETs are in a 20 mm × 20 mm. b) Output characteristics, c) transfer characteristics of FETs with graphene electrodes (L = 100 μm, W = 1000 μm). Output curves and black lines in the transfer curves were obtained using the patterning and transfer process (P–T process), as shown in Figure 3a. The red lines in the transfer curves were obtained by following the transfer and patterning process (T–P process) in Figure 1a. Inset of (b) shows schematic diagram of a cross section of FETs. Inset of (c) shows digital camera image of pentacene FETs displaying the flexibility and transparency. d) AFM image of PVP and a 50 nm-thick pentacene film on PVP following the T–P process. e) AFM image of PVP and a 50 nm thick pentacene film on PVP following the P–T process.

For this reason, pentacene films grown on PVP in the T–P process exhibited small grains with loosely packed inter-grain connectivity. To avoid these undesirable effects, we designed a new process in which graphene films were patterned on a copper foil, and patterned graphene electrodes were subsequently transferred using a polymer supported transfer method (P–T process, Figure 3a). In this process, RIE was performed on the Cu foil. Thus, the PVP surface, which is an important interface for charge transport, remained undamaged and yielded an RMS roughness of 0.6 nm, as confirmed by AFM (Figure 3e). Consequently, pentacene grew well on this smooth PVP layer and exhibited a grain size of ≈500 nm. Figure 3b shows the output curves corresponding to flexible pentacene FETs fabricated by the P–T process, which were well-behaved in the linear and saturation regimes. An average field-effect mobility of 0.12 $cm^2\ V^{-1}\ s^{-1}$ (over 15–20 devices) was obtained from the transfer curve, which exceeded that of FETs fabricated by the T–P process by more than an order of magnitude (Figure 3c). Because the overall procedure, including patterning and transfer of the graphene film, was performed at room temperature, carbon-based organic transistors with monolayer graphene electrodes were successfully fabricated on plastics substrates, and the devices exhibited excellent electrical properties with flexibility and transparency, as shown in Figure 3a,c, insets and SI, Figure S8.

In conclusion, we have successfully fabricated high-performance pentacene FETs with graphene source/drain electrodes by transferring and patterning CVD-grown monolayer graphene films. Systematic studies of the contact characteristics between source/drain electrodes and pentacene films

revealed that our patterned graphene electrodes exhibited properties that were superior to those of common metal electrodes. By designing a new process (patterning of graphene on a Cu foil) for the fabrication of patterned graphene electrodes, transparent/flexible organic transistors employing graphene electrodes were successfully assembled on plastics substrates with excellent performance properties. Monolayer graphene, with a high transparency and good conductivity, provides an alternative electrode material for use in next-generation flexible electronic devices assembled on plastic substrates.

Experimental Section

Materials and Device Fabrication: For the growth of graphene, copper foil was heated to 1000 °C with flowing 8 standard cubic centimeters per minute (sccm) H_2 at 90 mtorr (1 Torr ≈ 133 Pa) and subsequently CH_4/H_2 gases were flowed at 460 mtorr with rates of 24 and 8 sccm for 30 min, respectively. Then, the quartz tube was rapidly cooled to room temperature under H_2 flow. CVD-grown monolayer graphene films on a copper foil were covered with PMMA (M_w = 240 kg mol^{-1}) and floated in an aqueous solution of 0.1 M ammonium persulfate ($(NH_4)_2S_2O_8$) solution. After all copper layers had been etched away, the graphene film with the PMMA support was transferred to a silicon substrate with a 300 nm SiO_2 layer (capacitance = 10.8 nF cm^{-2}). The graphene film remained on the silicon substrate after removing the PMMA support with acetone. UV lithography (using a AZ1512 photoresist from Micro Chemicals) was used to pattern the graphene electrodes with defined channel lengths and widths (L = 10, 20, 50, 100 μm; W = 1000 μm). Etching of the graphene film was performed by application of a RIE plasma (100 W) for 2 s. The SiO_2 surface was treated with hexamethyldisiloxane (HMDS), as described previously [17] and the lift-off technique was used to remove the photoresist.

Polyarylate (PAR, Ferrania Technologies) films were used as flexible plastic substrates for fabricating the carbon-based OFETs. A water-based ink of the conducting polymer, poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonic acid (PEDOT/PSS, Baytron P from Bayer AG), was spin-coated as a gate electrode onto each PAR film. Then, a dielectric layer 316 nm thick (capacitance = 11 nF cm^{-2}) was deposited by spin-coating (at ≈5000 rpm) the dimethylformamide solution comprising 8.8 wt% poly-4-vinylphenol (PVP, M_w = 20 000 g mol^{-1}) and 6.2 wt% poly(melamine-*co*-formaldehyde), methylated (PMF, M_w = 511 g mol^{-1}) onto the PAR sheet with subsequent cross-linking for 1 h at 180°C in a vacuum oven. The graphene source/drain contacts were prepared by one of two different procedures (T–P and P–T processes). Pentacene was deposited from a quartz crucible onto the substrates at a rate of 0.2 Å s^{-1}.

Characterization: The film morphologies were characterized by optical microscopy (Zeiss) and AFM (Digital Instruments Multimode). 2D-GIXD experiments were performed at the 4C2 beamline of the Pohang Accelerator Laboratory in Korea. The capacitance of the dielectric was determined using an Agilent 4284 precision LCR meter. Keithley 2636A semiconductor parameter analyzer was employed to study the current–voltage characteristics of the devices at ambient condition.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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[1] a) A. K. Geim, *Science* **2009**, *324*, 1530; b) M. J. Allen, V. C. Tung, R. B. Kaner, *Chem. Rev.* **2010**, *110*, 132.
[2] a) C. A. Di, D. C. Wei, G. Yu, Y. Q. Liu, Y. L. Guo, D. B. Zhu, *Adv. Mater.* **2008**, *20*, 3289; b) S. P. Pang, H. N. Tsao, X. L. Feng, K. Mullen, *Adv. Mater.* **2009**, *21*, 3488; c) C. G. Lee, S. Park, R. S. Ruoff, A. Dodabalapur, *Appl. Phys. Lett.* **2009**, *95*, 023304.
[3] R. R. Nair, P. Blake, A. N. Grigorenko, K. S. Novoselov, T. J. Booth, T. Stauber, N. M. R. Peres, A. K. Geim, *Science* **2008**, *320*, 1308.
[4] M. S. Xu, M. Nakamura, M. Sakai, K. Kudo, *Adv. Mater.* **2007**, *19*, 371.
[5] X. S. Li, W. W. Cai, J. H. An, S. Kim, J. Nah, D. X. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, R. S. Ruoff, *Science* **2009**, *324*, 1312.
[6] S. Bae, H. Kim, Y. Lee, X. F. Xu, J. S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. R. Kim, Y. I. Song, Y. J. Kim, K. S. Kim, B. Ozyilmaz, J. H. Ahn, B. H. Hong, S. Iijima, *Nat. Nanotech.* **2010**, *5*, 574.
[7] A. Reina, X. T. Jia, J. Ho, D. Nezich, H. B. Son, V. Bulovic, M. S. Dresselhaus, J. Kong, *Nano Lett.* **2009**, *9*, 3087.
[8] a) C. D. Dimitrakopoulos, P. R. L. Malenfant, *Adv. Mater.* **2002**, *14*, 99; b) K. Asadi, Y. Wu, F. Gholamrezaie, P. Rudolf, P. W. M. Blom, *Adv. Mater.* **2009**, *21*, 4109.
[9] M. Ishigami, J. H. Chen, W. G. Cullen, M. S. Fuhrer, E. D. Williams, *Nano Lett.* **2007**, *7*, 1643.
[10] a) S. Unarunotai, Y. Murata, C. E. Chialvo, H. S. Kim, S. MacLaren, N. Mason, I. Petrov, J. A. Rogers, *Appl. Phys. Lett.* **2009**, *95*, 202101; b) S. Unarunotai, J. C. Koepke, C. L. Tsai, F. Du, C. E. Chialvo, Y. Murata, R. Haasch, I. Petrov, N. Mason, M. Shim, J. Lyding, J. A. Rogers, *ACS Nano* **2010**, *4*, 5591.
[11] a) D. Knipp, R. A. Street, A. Volkel, J. Ho, *J. Appl. Phys.* **2003**, *93*, 347; b) W. Kalb, P. Lang, M. Mottaghi, H. Aubin, G. Horowitz, M. Wuttig, *Synthetic Met.* **2004**, *146*, 279.
[12] a) D. H. Kim, H. S. Lee, H. C. Yang, L. Yang, K. Cho, *Adv. Funct. Mater.* **2008**, *18*, 1363; b) H. S. Lee, D. H. Kim, J. H. Cho, M. Hwang, Y. Jang, K. Cho, *J. Am. Chem. Soc.* **2008**, *130*, 10556.
[13] N. Koch, A. Vollmer, I. Salzmann, B. Nickel, H. Weiss, J. P. Rabe, *Phys. Rev. Lett.* **2006**, *96*, 156803.
[14] P. V. Necliudov, M. S. Shur, D. J. Gundlach, T. N. Jackson, *Solid-State Electron.* **2003**, *47*, 259.
[15] G. B. Blanchet, C. R. Fincher, M. Lefenfeld, J. A. Rogers, *Appl. Phys. Lett.* **2004**, *84*, 296.
[16] Q. Cao, Z. T. Zhu, M. G. Lemaitre, M. G. Xia, M. Shim, J. A. Rogers, *Appl. Phys. Lett.* **2006**, *88*, 113511.
[17] J. A. Lim, W. H. Lee, D. Kwak, K. Cho, *Langmuir* **2009**, *25*, 5404.