

# All Graphene-Based Thin Film Transistors on Flexible Plastic Substrates

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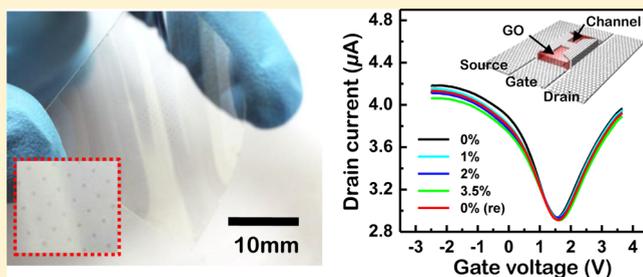
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## S Supporting Information

**ABSTRACT:** High-performance, flexible all graphene-based thin film transistor (TFT) was fabricated on plastic substrates using a graphene active layer, graphene oxide (GO) dielectrics, and graphene electrodes. The GO dielectrics exhibit a dielectric constant (3.1 at 77 K), low leakage current (17 mA/cm<sup>2</sup>), breakdown bias (1.5 × 10<sup>6</sup> V/cm), and good mechanical flexibility. Graphene-based TFTs showed a hole and electron mobility of 300 and 250 cm<sup>2</sup>/(V·s), respectively, at a drain bias of -0.1 V. Moreover, graphene TFTs on the plastic substrates exhibited remarkably good mechanical flexibility and optical transmittance. This method explores a significant step for the application of graphene toward flexible and stretchable electronics.

**KEYWORDS:** Graphene, graphene oxide, flexible electronics, thin film transistor



Graphene presents great promise as an active layer in field effect transistors owing to its exceptional electronic and optoelectronic properties.<sup>1–6</sup> Considerable efforts have been made in the last couple of years to improve their performance for high-speed radio frequency transistors.<sup>7–9</sup> Further, recent reports demonstrate successfully the integration of graphene thin film transistors (TFTs) on flexible plastics or even on stretchable rubbers.<sup>10–14</sup> To achieve such applications, the development of optimized gate dielectrics for a graphene active layer is critical. Nevertheless, the development of gate insulator materials that can achieve high-performance device operation, good mechanical properties, and low-temperature fabrication is not well established because graphene thin film is very sensitive to surface conditions of dielectric layers.<sup>15</sup> For example, oxides based high *k* dielectric materials, such as Al<sub>2</sub>O<sub>3</sub>, HfO<sub>2</sub>, and ZrO<sub>2</sub>, are the most widely used in graphene TFTs.<sup>16,17</sup> They have, however, several limitations including low-facture strains less than 1%, high-temperature process that cannot be used on plastic substrates, and poor interface between graphene and dielectric layers.<sup>18,19</sup> Hexagonal boron nitride (h-BN) materials have been also used in a bottom gate configuration as they can provide an atomically smooth surface that can protect the surface charge traps and the rippling of transferred graphene films.<sup>20</sup> The difficulty in synthesizing high-quality and large area h-BN films, however, limits some applications. Recently, as an alternative, graphene oxide (GO), which can be produced by the oxidation process of graphene in the same way as native oxide of Si, SiO<sub>2</sub>, has been exploited as a gate dielectric for

graphene-based TFTs. This material with good mechanical and optical properties offers a unique advantage for high-performance flexible and transparent electronic devices because it can be formed on a graphene channel by solution-based or direct oxidation process at room temperatures.<sup>21,22</sup> In particular, Jeong and co-workers reported that a GO insulator in an electronic device can be operated with good environmental stability.<sup>23</sup>

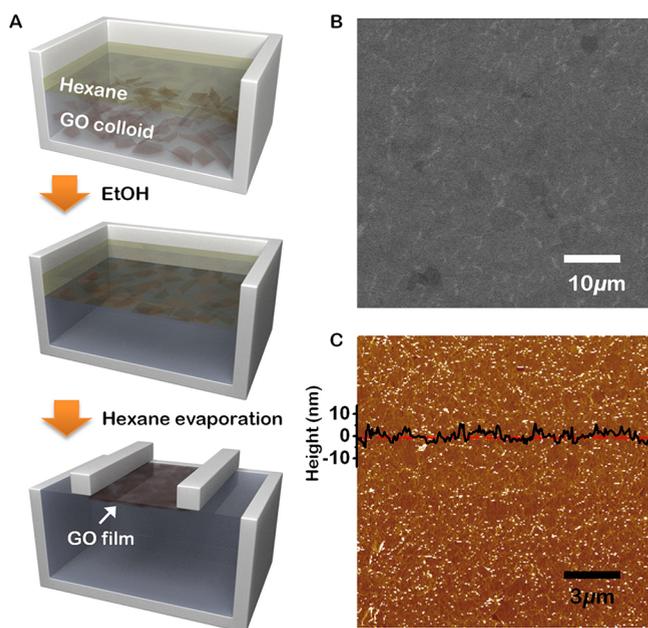
Although several recent studies report the fabrication of graphene transistor on a rigid substrate using GO flakes, significant challenges remain in the fabrication of graphene devices that meet mechanical and optical specification demands for flexible and transparent electronics.<sup>24</sup>

In this Letter, we present a promising method for the fabrication of an all graphene-based TFTs array on a flexible plastic substrate by utilizing the GO as the gate dielectric. The GO dielectric films can be easily formed over large areas at room temperature and exhibit a dielectric constant of 3.1 at 77 K. Furthermore, all graphene-based TFTs fabricated on plastic substrates show very good mechanical flexibility and optical transmittance.

A schematic diagram for the preparation of two-dimensional GO films is represented in Figure 1A. The GO flakes in an

**Received:** March 9, 2012

**Revised:** May 30, 2012



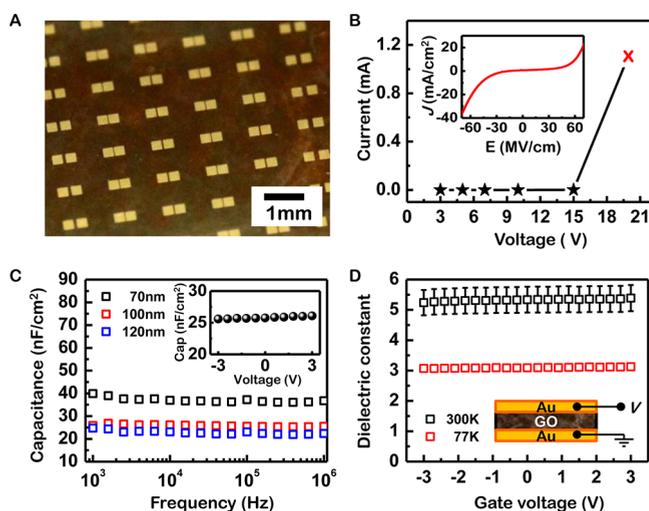
**Figure 1.** (A) Schematic of the GO film formation process at the hexane/water interface. Pinhole-free multilayered GO structure can be formed by repeating this LB process. (B,C) SEM and AFM images showing large area, layer-by-layer assembly of GO films with uniform coverage. The measured surface profile was about  $\pm 5$  nm, which may be caused by folding and wrinkling of the GO flake.

aqueous phase are inherently stabilized by the negatively charged functionalities, such as hydroxyl, carbonyl, and carboxyl moieties. An immiscible water/oil interface was formed by pouring hexane on the water surface, and ethanol was then added slowly to the surface of the water/hexane layer by using a mechanical syringe pump, resulting in GO trapping at the interface. This process is very similar to the metal nanoparticle entrapment at the water/oil interface.<sup>25</sup> The dielectric constant of water decreases when a miscible solvent with a lower dielectric constant, such as ethanol, is added. The surface charge of the GO flakes gradually decreases in proportion to the amount of added ethanol. The decrease in interfacial energy at the water/hexane interface by the adsorption of GO flakes is thought to be the driving force for the entrapment of GO flakes, as the charge separation ability of water is reduced by the ethanol addition. The spontaneous evaporation of hexane leaves the two-dimensional GO films floating on the top of the water surface. Sparsely floating GO flakes can be assembled into one large close-packed film by decreasing the surface area using two Teflon bars. The close-packed GO films could then be transferred by horizontal lifting to a substrate. Finally we stacked pinhole-free multilayered GO structures by repeating the Langmuir–Blodgett (LB) method.

The quality of the GO film was analyzed using Raman spectroscopy and X-ray photoelectron spectroscopy (XPS) (see Supporting Information, Figure S1). In the Raman spectrum of GO, the G band is broadened and up-shifted to  $1599\text{ cm}^{-1}$ , which is caused by the presence of an isolated double bond during the oxidation process, and the D peak is located at  $1363\text{ cm}^{-1}$ .<sup>26</sup> The decomposition of XPS peaks shows the existence of the oxygen-containing groups on the graphene surface such as C=O, O–C=O, and C–O bonds. A scanning electron microscopy (SEM) image showed layer-by-layer assembly of GO film with a few centimeter dimension (Figure 1B). Large

areas of GO layers can be formed in an uniform coverage due to the stable dispersion against flocculation or coagulation, which is an advantage of the LB method.<sup>27</sup> The GO film surface was further examined by atomic force microscopy (AFM), which confirms the SEM observation. Image taken by AFM proves very smooth and pinhole-free surface morphology from overpacked GO film (Figure 1C). As shown in the line scans, the surface roughness is 5 nm, which originated from folds or wrinkles at GO flake edge. Previous studies reported that the roughness of GO was measured to be around 1 nm and that overlapped edges were usually near 2 nm.<sup>27,28</sup>

To elucidate the GO as gate dielectric material, we sandwiched well-oriented GO film between Au electrodes. The GO film thickness was measured by AFM at the edge of the film. Top electrode arrays (from  $5 \times 5$  to  $300 \times 300\ \mu\text{m}^2$ ) were formed by Au deposition and lift off methods (Figure 2A).



**Figure 2.** (A) GO capacitor (Au/GO/Au) on the insulating substrate. Dimension of top electrode is from  $5 \times 5$  to  $300 \times 300\ \mu\text{m}^2$ . (B) Dielectric breakdown of the GO layer. Inset shows the two terminal  $I$ – $V$  characteristics of the GO films at room temperature. (C) The frequency dependence of the capacitance at 77 K. Inset shows capacitance–voltage measurement of the GO film with 100 nm thickness. (D) The bias-dependent dielectric constant curves at different temperatures.

Before measurements, GO capacitor devices with the metal–insulator–metal structure were placed in a high-vacuum chamber ( $\sim 1 \times 10^{-6}$  Torr) for 12 h to minimize the potential charge trap sites which absorb in GO film (see Supporting Information, Figure S2).<sup>29</sup> First we investigated the insulating property, an important concern with any gate dielectric material, of GO films when a bias voltage was applied between the top and the bottom electrodes.<sup>30</sup> The inset of Figure 2B shows the bias-dependent leakage current of the GO thin films ( $t \sim 100$  nm) at room temperature. An insulating state was observed on the different thicknesses of the GO capacitor, and the leakage current density was  $17\text{ mA/cm}^2$  at a bias field of 50 MV/cm (see Supporting Information, Figure S3). The breakdown strength of GO, which is important for device applications, was also investigated with an electric field. When a bias voltage exceeds 15 V, the current through the GO became unstable, and the corresponding breakdown electric field was  $1.5 \times 10^6\text{ V/cm}$  (Figure 2B). The stability of GO film was tested under room temperature over  $10^5$  s. Dry nitrogen ( $\text{N}_2$ ) conditions kept the insulating property of GO stable. On the

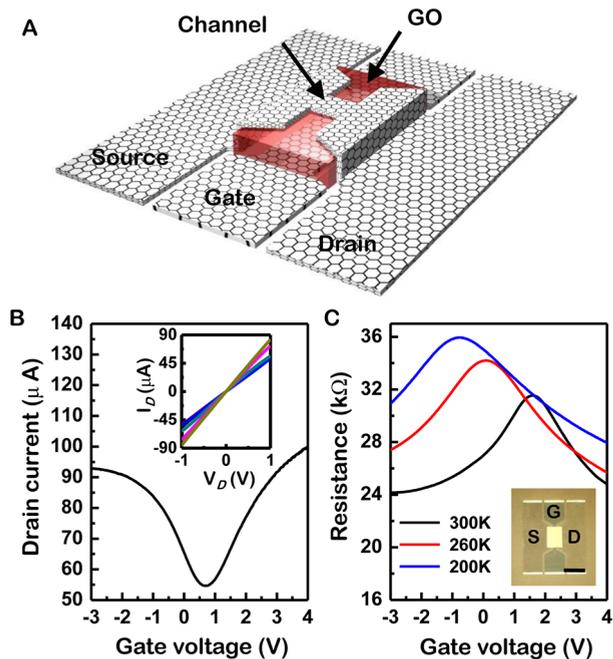
other hand, ambient conditions caused a leakage current after  $10^4$  s, which resulted from the degradation of GO film by absorbed water molecule. We believe that this degradation can be evaded through the passivation layer (see Supporting Information, Figure S2). Figure 2C shows the capacitance value, normalized to  $1 \text{ cm}^2$ , for the GO as function of frequency from 1 kHz to 1 MHz at  $T = 77 \text{ K}$  (Solartron SI-1260 impedance/gain-phase analyzer, the supplied ac voltage of 0.1 V). The capacitance of a pure GO film measured at 1 kHz was 41, 27, and 25 nF/cm<sup>2</sup> at thicknesses of 70, 100, and 120 nm, respectively, without dielectric dispersion up to 1 MHz. The capacitance of GO film exhibited stable operation without remarkable change up to a voltage bias of 3 V (inset of Figure 2C). The dielectric constant of GO capacitors with bias voltage at different temperatures is also depicted in Figure 2D. At  $T = 77 \text{ K}$ , the dielectric constant was 3.1 and independent of the bias voltage at several thicknesses but increased up to 5 at room temperature (see Supporting Information, Figure S4). This difference can be interpreted by several kinds of defects, including mobile ionic defects and space charges induced during the oxidation process of graphene.<sup>31,32</sup> Although the GO films may contain ionic impurities, it might be possible to improve the dielectric properties through optimized purification process.

We built a bottom-gated graphene thin film transistor with the GO gate dielectric layer (Figure 3A). In the first step, high-quality monolayer graphene films were grown on Cu foils by chemical vapor deposition and transferred onto a SiO<sub>2</sub>/Si wafer using a method described in previous studies.<sup>5,33</sup> The gate patterns of the graphene films were formed by photo-

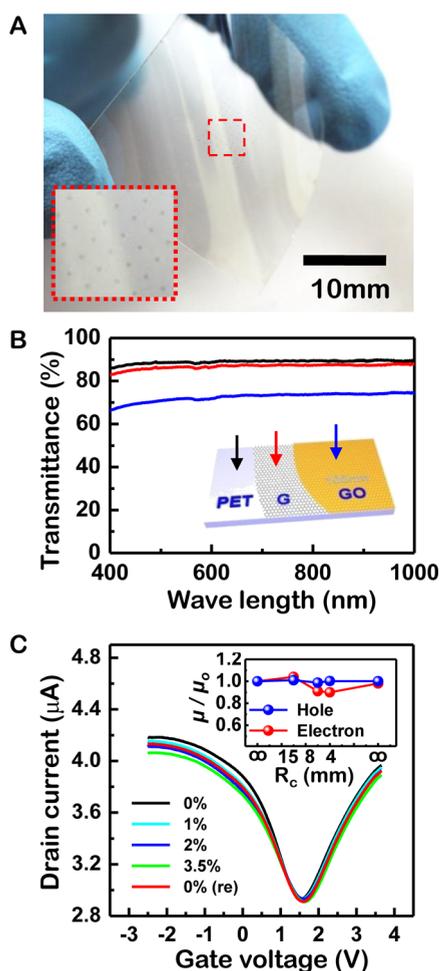
lithography and reactive ion etching (RIE) with O<sub>2</sub> plasma. GO gate dielectric layer (100 nm thick) was repeatedly formed by LB method over the gate dielectric area patterned by photoresist. After drying under ultrahigh vacuum, the photoresist was removed. The monolayer of graphene working as the channel was transferred onto the GO and patterned in the same way as the previous process. The source (S)/drain (D)/channels were monolithically patterned from graphene film without the use of traditional metal electrodes. The monolithic devices have obvious advantages including good optical transmittance, simple device design, and improved contact at the channel-to-S/D interface. Figure 3B shows the electronic transfer and output characteristics of a monolayer graphene transistor on a GO dielectric layer (channel widths of 25 μm and lengths of 10 μm). Electrical testing was performed by using a Keithley 4200-SCS semiconductor analyzer at room temperature in high vacuum ( $\sim 1 \times 10^{-6}$  Torr). The Dirac voltage, corresponding to the overall charge neutrality points, occurred at positive voltage, which means graphene channel was lightly p-doped by acceptor. Although graphene-based TFTs show low on-off current ratio ( $I_{\text{on}}/I_{\text{off}} \sim 1.8$ ) due to the intrinsic property of zero-band gap of graphene, the hole and electron field effect mobilities were 300 and 250 cm<sup>2</sup>/(V·s) at  $V_D = -0.1 \text{ V}$ , respectively. The devices exhibit better mobility than those of graphene-based TFT built through different fabrication methods (see Supporting Information, Table S1). The inset of Figure 3B shows output characteristic ( $I_D - V_D$ ) of the GO-insulated graphene TFTs at six different gate voltages from -1 to 1 V. The device exhibited a clear increase in the conductance induced by the gate voltage and completely linear behavior, which is typical for zero band gaps. The temperature dependence of the resistance at monolayer graphene is shown in Figure 3C. We note that the resistance linearly increases and shifts toward the negative gate voltages with decreasing temperature. Kim and Fuhrer suggested that longitudinal acoustic (LA) phonon scattering gives rise to a linear resistivity independent of carrier density expressed by the following equation:<sup>34,35</sup>

$$\Delta\rho = \frac{\pi D^2 k_B T}{4e^2 \hbar \rho_m v_F^2 v_{\text{ph}}^2}$$

where  $D$  is the deformation potential,  $k_B$  is the Boltzmann constant,  $\rho_m = 7.6 \times 10^{-7} \text{ kg/m}^2$  is the graphene mass density,  $v_{\text{ph}} = 2 \times 10^4 \text{ m/s}$  is LA phonon velocity, and  $v_F = 1 \times 10^6 \text{ m/s}$  is Fermi velocity. In addition, the negative shift of resistance at low temperatures was attributed to the n-doping effect from GO. Although electronic transport properties exhibited p-doping with the Dirac point at the positive gate voltage at room temperature, the Dirac point gradually moved toward zero and finally exhibited n-doped graphene behavior according to the temperature decrease. Indeed, the n-doped behavior was an intrinsic characteristic of graphene on GO which has electron-rich oxygen atoms (from carbonyl and epoxy functional groups) working as an electron donor. However, the remaining water absorption in GO and graphene dominantly affects the transfer characteristic by thermal vibration over 100 K.<sup>36,37</sup> Large phonon densities at high temperatures by the water absorption of GO cause the p-doping effect on the graphene channel, which can be proved by the temperature dependence of the hysteresis loop (see Supporting Information, Figure S5).<sup>38</sup>



**Figure 3.** (A) Schematic illustration of bottom-gated graphene/GO transistor. The graphene channel which was monolithically patterned with source and drain electrodes is above the GO dielectric. (B) Typical transfer characteristic of graphene/GO transistors, indicating the hole and electron mobilities are 300 and 250 cm<sup>2</sup>/(V·s) at  $V_D = -0.1 \text{ V}$ , respectively. (C) Resistance versus applied gate voltage at different temperatures. Inset shows the microscope image of the real device that has a channel length ( $L_c$ ) of 10 μm and width ( $W_c$ ) of 25 μm, respectively (scale bar: 100 μm).



**Figure 4.** (A) Optical image of the all-graphene-based transistor formed on plastic substrate. (B) Optical transmittance spectra as function of wavelength for the PET substrate (black line), through monolayer graphene (red line) and GO dielectrics (blue line) of the device including PET substrate. (C) Transfer curves measured as a function of tensile strains (from 0% to 3.5%). Inset shows effective mobility as a function of the bending radius.

Figure 4A shows the completed array of the all-graphene-based TFTs on a plastic substrate. The rectangle indicates the GO dielectric layer which is slightly visible as arrays of gray squares in the center of this image. Figure 4B presents optical transmission spectra of the entire graphene/GO TFT including the plastic substrate. The transmittance was reduced by  $\sim 16\%$  in the TFT with the monolayer graphene electrode/channel and 100 nm-thick GO dielectric layer, exclusive of the bare PET substrate (88%) at a wavelength of  $\lambda = 550$  nm. The transmittance is comparable to that of the oxide material-based devices, such as ZnO and IGZO<sup>39,40</sup> (see Supporting Information, Figure S6). The devices on PET show a little degraded electrical properties, compared with those on rigid substrates due to the effect of the surface morphology of plastic substrate (Figure 4C).<sup>20</sup> Devices over 70% ( $\sim$  total 64 ones) exhibit stable operations, and the Gaussian fit indicates a hole and electron mobility of 150 and 116  $\text{cm}^2/(\text{V}\cdot\text{s})$ , respectively, at a drain bias of  $-0.1$  V (see Supporting Information, Figure S7). We suppose that the failure of devices mainly results from the defects of the GO film.

High-strain endurable devices should have two main properties: (i) mechanically flexible components and (ii)

mechanically and electrically tight bonding between each layer. We tested the flexibility of transistors by bending the supporting PET substrate using a setup described elsewhere.<sup>41</sup> The bending properties of the devices are also very good, as expected, due to the excellent mechanical properties of both graphene and GO (Figure 4C).<sup>22,42</sup> Typical transfer characteristics were quite stable under the operation of tensile strains from 0 to 3.5% (corresponding to bending radii calculated using models for this geometry of 4.13 mm) and showed complete recovery after the strain was relaxed. The normalized hole and electron mobility had a distribution of less than 10% (inset of Figure 4C).

In summary, flexible, transparent, monolithic graphene-based devices were realized by utilizing GO as a dielectric and graphene as both a semiconducting channel and an electrode via a low-temperature printing process. This all-graphene-based device provides an important viable route to future electronic devices requiring mechanically flexible, transparent, high-performance, and low-voltage operation.

## ■ ASSOCIATED CONTENT

### 📄 Supporting Information

Detailed analysis information and statistical data. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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### Notes

The authors declare no competing financial interest.

## ■ ACKNOWLEDGMENTS

This work was supported by the Basic Research Program and Global Frontier Research Center for Advanced Soft Electronics through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (20090083540, 20090092809, 2012006049, and 20110031635) and the IT R&D program of Ministry of Knowledge Economy of Korea (2008-F024-02, Development of Mobile Flexible Input/Output Platform). S.P. acknowledges the support by the World Class University program (R31-2008-10029).

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