Large-area graphene synthesis and its application to interface-engineered field effect transistors

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ABSTRACT

This article reviews recent advances in the large-area synthesis of graphene sheets and the applications of such sheets to graphene-based transistors. Graphene is potentially useful in a wide range of practical applications that could benefit from its exceptional electrical, optical, and mechanical properties. Tremendous effort has been devoted to overcoming several fundamental limitations of graphene, such as a zero band gap and a low direct current conductivity-to-optical conductivity ratio. The intrinsic properties of graphene depend on the synthetic and transfer route, and this dependence has been intensively investigated. Several representative reports describing the application of graphene as a channel and electrode material for use in flexible transparent transistor devices are discussed. A fresh perspective on the optimization of graphene as a 2D framework for crystalline organic semiconductor growth is introduced, and its effects on transistor performance are discussed. This critical review provides insights and a new perspective on the development of high-quality large-area graphene and the optimization of graphene-based transistors.

1. Introduction

Graphene has been extensively studied over the past several years for its utility in a variety of research fields, including physics, chemistry, biology, and several engineering fields, including electrical, mechanical, and materials engineering. This two-dimensional carbon allotrope with a planar honeycomb lattice displays exceptional physical properties, such as ultrahigh electrical and thermal conductivities, excellent mechanical strength, anomalous quantum Hall effect, and Klein tunneling [1–8]. The fascinating electrical and mechanical properties of graphene have attracted considerable attention on the material as a potential basis material in post-silicon semiconductor technologies [9–12].

A major focus of experimental research has been the development of new synthetic routes to the high-quality controlled production of layered graphene sheets. The most commonly employed methods are micromechanical [13] and chemical exfoliation of graphite [14], reduction of graphite oxide [15,16], epitaxial growth on SiC [17], and chemical vapor deposition (CVD) on transition metals [18,19]. With the help of these synthetic approaches, graphene has yielded significant utility in the fabrication of touch panels, transistors, solar cells, molecular sensors, supercapacitors, radio-frequency integrated circuits, and soft electronics [20].

With the goal of facilitating application development, recent studies have attempted to prepare uniform large-area graphene sheets. Because graphene displays a high chemical sensitivity [21], its electrical and optical properties are highly sensitive to the chemical environment, including the substrate properties or the presence of chemicals in contact with graphene [22,23]. To this end, the preservation of the intrinsic properties of graphene during the synthesis and transfer processes has been an important consideration for the development of large-area graphene synthetic approaches. For a variety of applications, overcoming the intrinsic limitations, such as the zero band gap of graphene, the low ratio of direct current (DC), and the low optical conductivity, poses a significant challenge to the development of graphene-based electronics [24].

In this review, we discuss several representative works related to the large-area synthesis of graphene and its application to field-effect transistor (FET) devices. The first section briefly reviews chemical vapor deposition (CVD) methods used to produce large-area graphene with special attention to the electrical and mechanical properties of the synthesized graphene films. We next review reports describing the efforts that have been applied toward overcoming the fundamental limitations of graphene and

the use of graphene as channel and electrode materials in FETs. Finally, concluding remarks and a perspective on future research in the field are provided.

2. Large-scale synthesis of graphene

CVD methods have, in recent years, shown promise toward achieving the large-area growth of graphene and its use in the preparation of macroscopic highly conducting transparent electrodes for use in flexible and stretchable electronics. The development of large-scale graphene growth has been achieved not only by scaling up CVD equipment, but also using advanced methods for etching metal layers and transferring isolated graphene films to other substrates.

Fig. 1 shows several photographs of graphene films synthesized by CVD methods via a gradual scale-up progress that increased the sample dimensions from 1 to 30 in. [25–28]. Kim et al. suggested the transfer of a centimeter-scale graphene film grown on a Ni (300 nm)/SiO$_2$ (300 nm)/Si substrate using a PDMS stamp (Fig. 1(a)). This substrate was placed in a quartz tube under a reactive gas mixture containing CH$_4$/H$_2$/Ar atmosphere. The temperature was increased to 1000 °C followed by rapid cooling to room temperature. The thin Ni layer was etched using FeCl$_3$ (or acids) within a few minutes, and the isolated graphene film was transferred using poly(dimethylsiloxane) (PDMS) stamps, enabling the production of patterned graphene films. The etching process was improved using a mechanical peel-off step to simply remove the metal layer. Fig. 1(b) shows wafer-scale high-quality graphene films as large as 3 in. in dimension (wafer size), developed on Ni and Cu films under ambient pressure. The graphene films could be transferred onto any substrate by instantaneously etching the metal layers [29]. The graphene and metal layers supported by a polymer film, such as a soft PDMS stamp or a thermal-release tape, could be mechanically separated from the SiO$_2$/Si wafer. This process permitted the rapid etching of metal and the successful isolation of graphene. The wafer-scale graphene films could be transferred to arbitrary substrates then patterned using conventional lithography.

These techniques removed the limitation of graphene growth to rigid substrates. Large flexible copper foils could be used not only to maximize the scale of the CVD-based graphene and to provide good homogeneity and reproducibility of the graphene growth (Fig. 1(c)). The 30 in.-scale graphene films set a new record for the largest graphene film grown to date via a roll-to-roll process. Initially, a roll-type graphene film, grown on a copper foil, was attached to a thin polymer film coated with an adhesive layer by passing between two rollers [28]. The copper foil was etched using an aqueous 0.1 M ammonium persulfate solution (NH$_4$)$_2$S$_2$O$_8$. The graphene films were detached from the thermal release tape polymer support, followed by transfer onto a transparent flexible target substrate, such as a PET film. The efficient transfer and chemical doping of the graphene films improved the electrical and optical properties of the single-layer graphene sheets. The ultra-large-area synthesis and roll-to-roll production of graphene, therefore, provides improved scalability and
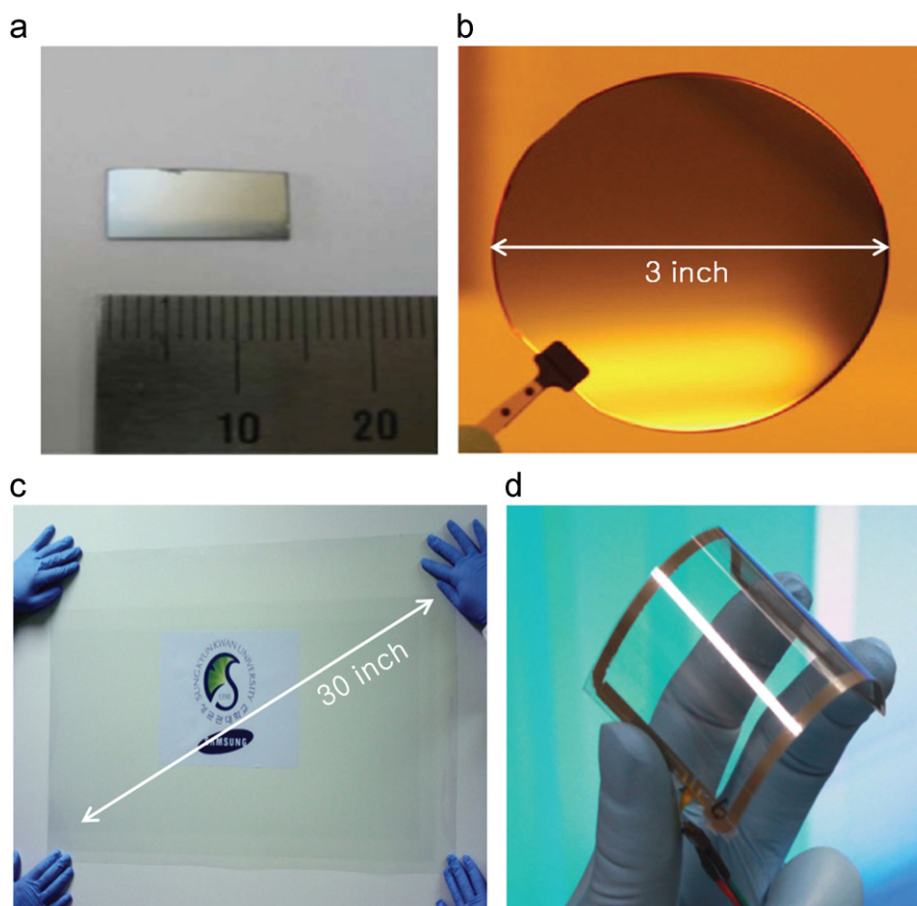
Fig. 1. (Color online) T**he graphene scale-up by process via CVD.** (a) A centimeter, (b) wafer-scale graphene film grown on Ni(300 nm)/SiO$_2$ (300 nm)/Si substrate. (c) a transparent ultralarge-area graphene film transferred on a 35-inch PET sheet. (d) an assembled graphene/PET touch panel showing outstanding flexibility. (Reproduced from Ref. [25] with permission from American Chemical Society, Ref. [26], Ref. [28] with permission from Nature Publishing Group, and Ref. [27] with permission from AAAS).

processability of graphene films for use in macroscopic devices and flexible/stretchable electronics. For example, graphene-based touch-screen devices have been demonstrated, revealing a high flexibility and conductivity (Fig. 1(d)). The continuous production of graphene-based electronic devices over large scales facilitates the use of graphene transparent electrode materials as a replacement for ITO [30–34].

Fig. 2 shows the optical and electrical characterization of CVD-based graphene films. The optical transmittance gradually decreased by 2.2%–2.3% in the graphene films prepared using layer-by-layer transfer on a quartz substrate (Fig. 2(a)). The measured optical transparency of 97.4% for a single layer agreed well with the previously reported value of a mechanically exfoliated monolayer [35]. The right inset shows optical images with different numbers of stacked layers. The uniform changes in the transmittance indicate that the average film thickness was a monolayer [36]. Fig. 2(b) shows the Raman spectra of CVD-grown graphene films with different numbers of stacked layers. The left inset shows a photograph of the graphene layers transferred onto a 4 in. SiO$_2$ (300 nm)/silicon wafer. The intensities of the G- and 2D band peaks increased in a constant ratio as the number of layers increased. This observation could be explained in terms of the random orientations of the hexagonal lattices between any pair of layers. By contrast, the layer-by-layer stacking of graphene exfoliated from graphite crystals was aligned. As a result, the 2D/G band intensity ratio was not constant. The results revealed

that the electronic band structures and the overall conductivity of the graphene films formed by a monolayer were preserved, even in stacked multilayers [17].

Interestingly, the quantum Hall effect could be observed in the CVD-grown graphene (Fig. 2(c)). The longitudinal (R_{xx}) and transverse (R_{xy}) magnetoresistance values were measured under a high magnetic field of 8.8 T. The monolayer graphene quantum Hall effect was clearly observed, revealing a plateau with a fill factor of $\nu = 2$ at $R_{xy} = (2e^2/h)^{-1}$ and a zero value in R_{xx} (Here, e is the elementary charge and h is Planck's constant.) The quantum Hall plateaus (the horizontal dashed lines) developed for higher fill factors. The electrical properties of the monolayer graphene devices revealed half-integer quantum Hall effects and a high electron mobility of 3750 cm^2 V^{-1} S^{-1}. These results demonstrated that the quality of the CVD-grown graphene was comparable to the quality of mechanically exfoliated graphene [1,37].

Fig. 2(d) shows the resistance of a CVD-grown graphene film transferred to a PDMS substrate, measured under an isotropic stretching force of 0%–30%. The resistance was stable until a stretching force of 12%, indicating the maximum stretching range. The left inset corresponds to the case in which a graphene film was transferred to an unstretched PDMS substrate. The properties revealed stable properties under cyclical stretching. The longitudinal and transverse resistances (R_y and R_x) appeared to be stable up to a stretching factor of 11% and varied by only one order of magnitude at 25% stretching. This excellent mechanical stability
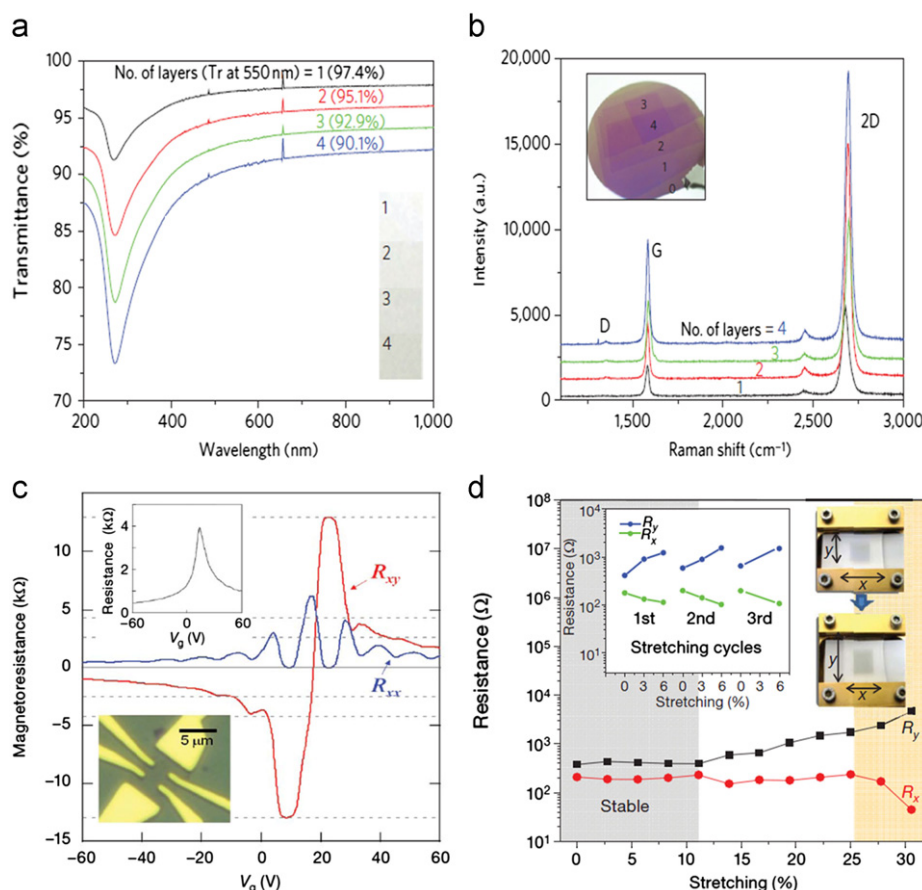

Fig. 2. (Color online) **Optical and electrical characterizations of the graphene films.** (a) UV–vis spectra of layer-by layer transferred graphene on quartz substates. The inset shows optical images for the different number of layers (1 × 1 cm^2). (b) Raman spectra of graphene films with different numbers of stacked layers. The inset shows an image of transferred graphene layers on a 4-inch SiO$_2$ (300 nm)/silicon wafer. (c) Electrical properties of monolayer graphene devices showing the half-integer quantum Hall effect and high electron mobility. The upper inset shows a four-probe electrical resistance measurement on a monolayer graphene Hall bar device (lower inset) at 1.6 K. (d) Resistance change of a transferred graphene film on PDMS substrate stretched by ∼12%. The left inset shows the case in which the graphene films in transferred to an unstretched PDMS substate. The right inset shows the movement of holding stages and the consequent change in shape of the graphene film. (Reproduced from Ref. [35] with permission from AAAS, Ref. [36] with permission from American Chemical Society).

of the graphene was comparable to the stability of conventional materials used in stretchable electronics [38]. It has been suggested that the electronic band structure and sheet resistance of graphene may be varied (controlled) by applying a stretching force. These results show that the electromechanical properties of graphene permit the use of CVD-grown large-scale graphene in flexible and stretchable conducting transparent materials.

3. Graphene field-effect transistors

3.1. Field-induced mobility of CVD graphene

Graphene-based transistors have been fabricated on SiO_2/Si substrates to take advantage of (i) the optical contrast between monolayer graphene and SiO_2 and (ii) the feasibility of fabricating devices with conventional metal oxide–semiconductor structures [1,37,39]. The performances of graphene field-effect transistors (FETs) on SiO_2 substrates, however, are limited by charged impurity scattering, extrinsic surface phonon scattering, resonant scattering from atomic-scale defects, and corrugation or doping by residual adsorbents [40–43]. To overcome these performance limitations, several approaches, including graphene suspensions [44], the use of ultraflat h-BN substrates [45], and the insertion of a hydrophobic buffer layer between graphene and the substrate, have been introduced to yield high room-temperature field-effect mobilities up to 200,000 cm^2/Vs [46,47]. Table 1 summarizes the recent advances toward high field-effect mobilities in graphene layers on a variety of substrates.

Lee et al. described a systematic study in which the intrinsic doping levels of graphene could be restored by inserting a buffer layer between the graphene and the gate dielectric to modify the surface properties of the SiO_2 and, thereby, enhance the electrical properties of graphene FETs [46]. The chemical and physical properties of graphene/dielectric (SiO_2) interfaces were controlled by treating the SiO_2 substrates with hydrophobic self-assembled monolayers (SAMs) of hexamethylsilazane (HMDS) and two organoalkyl silanes, octyltrichlorosilane (OTS) and octadecyltrichlorosilane (ODTS), with various alkyl chain lengths (C8 and C18 respectively), as shown in Fig. 3(a). CVD-grown monolayer graphene was transferred from a copper foil to the substrate to evaluate the chemical and physical interactions between the graphene and various SAM-modified SiO_2 substrates. The effects of the SAM buffer layer on the electrical properties of the graphene films were examined by depositing Au source/drain electrodes directly onto the graphene films. Fig. 3(b) shows the variations in

Table 1
Recent advances in the field-effect mobility of graphene prepared via a variety of synthetic routes and on a range of substrates. The mobility values were calculated from the derivative of the Drude formula.

Synthetic route	Gate insulator (GI)	Carrier mobility (cm^2/Vs) @RT	Ref.
Mechanical exfoliation	Bottom GI: SiO_2	∼15,000	[39]
	Suspended sheet	200,000	[44]
CVD on copper	Bottom GI: SiO_2/h-BN[*]	25,000–140,000	[45]
	Bottom GI: SiO_2/ODTS[**]	∼47,000	[47]
	Bottom GI: SiO_2	4050	[27]
Decomposition of SiC	Top GI: SiO_2	5400	[79]
Reduced graphene oxide	Bottom GI: SiO_2	∼1 at low temperature	[4]

* h-BN: hexagonal boron nitride.
** ODTS: octadecyltrichlorosilane based self-assembled monolayers (SAMs).
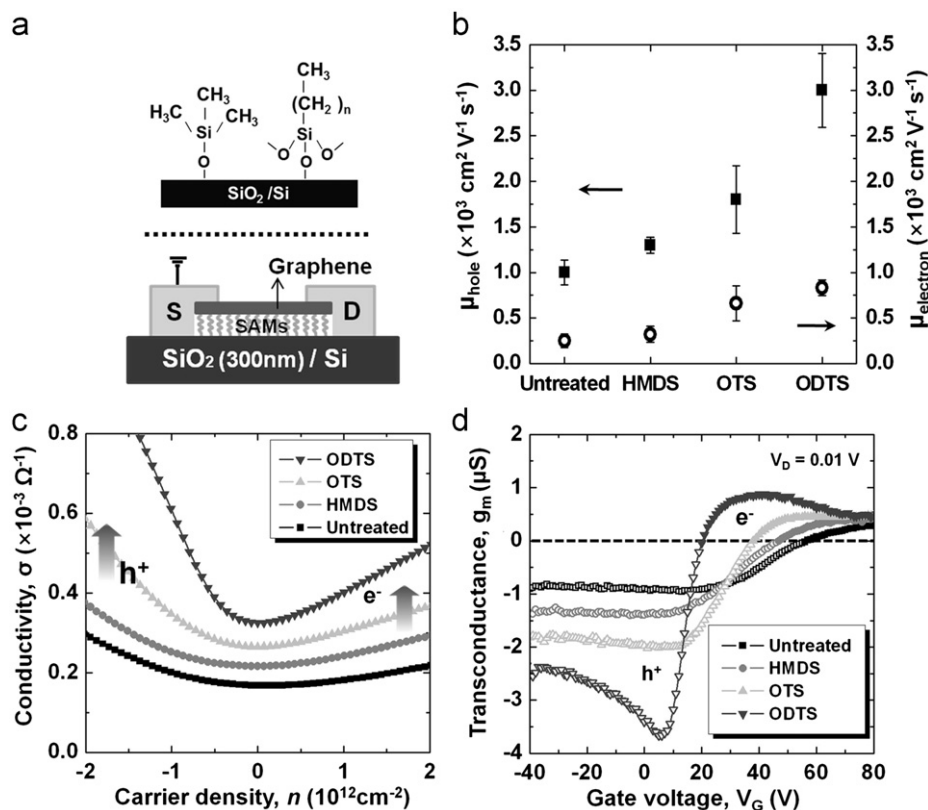

Fig. 3. Charged impurity scattering on monolayer graphene FETs. (a) Chemical structures of the HMDS-modified (top left) and organosilane-modified (top right) SiO_2/Si substrates (OTS for $n=7$ and ODTS for $n=17$) and a schematic diagram showing the graphene FETs with SAMs as buffer layers between graphene and substrate (bottom). (b) Comparative plots of electron and hole field-effect mobilities. (c) Detailed view of the density-dependent conductivity near the Dirac point. (d) Transconductance g_m of the graphene FETs on various SAM-modified SiO_2/Si substrates as a function of V_G. (Reproduced from Ref. [46] with permission from Wiley).

the field-effect mobilities upon increasing the alkyl chain length. The electron and hole mobilities calculated in the linear regime increased with increasing SAM alkyl chain length. The observed asymmetry in the hole and electron mobilities (Fig. 3(c)) could be attributed to the differences in the scattering cross-sections of the holes and electrons or to drift in the charged impurities from the substrate [48,49]. Because the surface roughness did not decrease after forming the SAMs on the SiO_2 substrates, the enhanced mobility was directly correlated with the effective screening of the SiO_2 surface. SiO_2 screening has previously been reported to limit the graphene mobility due to the presence of charged impurities [50,51]. As the density of charged impurities decreased, the FETs exhibited lower $V_{G,Dirac}$ values, higher hole/electron mobilities, higher minimum conductivities, and narrower plateau widths (Fig. 3(c)). Furthermore, the sublinear conductivity at high V_G, clearly observable in the transconductance (g_m) curve (Fig. 3(d)) of the ODTS-SAM, was correlated with the changes in the scattering mechanism from long-range scattering to short-range scattering. The electrical measurements confirmed that the SAMs with long alkyl chain lengths effectively screened the charge impurities originating from the adsorbents on the SiO_2 surface, thereby reducing the graphene doping and enhancing the electrical properties of the graphene FETs. Thus, appropriate surface chemistries at the graphene/substrate interfaces were essential for optimizing the intrinsic electrical properties of the graphene toward development of high-performance graphene transistors.

3.2. Band gap engineering of graphene for transistor applications

Graphene-based electronic devices have been designed to exhibit a high carrier mobility, an ultrahigh speed, large-scale flexibility, and molecular-scale sensitivity; however, due to the absence of a band gap, pristine graphene devices cannot be switched off, thereby posing a significant challenge to digital electronic device applications. To overcome this disadvantage, several approaches to enlarging the band gap in graphene have been tested, including fabricating graphene nanoribbons and implanting periodic heteroatoms on the graphene lattice [52–55]. On the other hand, bilayer graphene presents a unique alternative to band gap engineering because a perpendicular electric field may be applied to break the inversion symmetry of graphene [56–59]. For instance, gate-controlled tunable band gap bilayer graphene films have been successfully demonstrated by fabricating field-effect transistors (FETs) with dual-gate structures. The resultant band gap was nearly 250 meV, which corresponds to an on/off current ratio on the order of 10^2 [57]. Alternative purely chemical approaches for generating a built-in perpendicular electric field are also possible. Several researchers have reported that the presence of metal adatoms or molecular dopants with strong polarities can introduce an electric field onto the bilayer graphene and induce a band gap, thereby producing an on/off current ratio similar to that of dual gated transistors; however, because molecular dopants were applied only on one side of the bilayer graphene, the charge carrier density varied along with the band gap.

Park and Jo et al., reported the facile single-gate operation of band gap engineered graphene transistors in which the carrier density and band gap of the bilayer graphene were independently controlled via dual molecular doping [60]. Amine-functionalized SAMs were deposited onto the silicon substrate to control the n-doping behavior of the graphene on the bottom side, and 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F4-TCNQ; Fig. 1(b), top) was thermally deposited onto the bilayer graphene FETs to induce a doping-driven perpendicular electric field on the top side. F4-TCNQ consists of cyano and fluoro groups with electron-withdrawing characteristics; therefore, its low-lying

lowest unoccupied molecular orbital (LUMO) level occurs at -5.2 eV. This, in turn, leads to p-doping of the graphene upon contact between F4-TCNQ and the graphene. The position of the charge neutrality point (CNP, the location of maximum resistivity) of the dual-doped bilayer graphene could be manipulated by independently controlling the degree of doping on each side, for example, by varying the thickness of the F4-TCNQ layer. The resultant FET performance, as shown in Fig. 4(a) displayed an increase in the off resistance of up to 2 orders of magnitude, yielding a higher current on/off ratio compared to pristine bilayer graphene transistors, corresponding to an electrical band gap of nearly 150 meV. The optical band gap was estimated using infrared spectroscopy, which clearly showed a shift in the absorption peak near 200 meV with increasing F4-TCNQ layer thickness. The discrepancy between the electrical and optical band gaps could be explained by the tunneling of carriers through defect sites [58,61]. The position of the CNP and the resultant charge carrier density depended on the amount of effective doping, which could be derived from the compensation between the displacement fields exerted by the opposite types of dopants. The independent CNP position modulation resembled the dual gated graphene transistor behavior in which the displacement field from the top and bottom gates broke the inversion symmetry while keeping the graphene charge neutral.

Despite the successful demonstration of band gap opening via dual molecular doping, several challenges remain in the area of molecular doping homogeneity. As in the bilayer graphene devices, the single layer graphene devices showed an increase in the off resistance with the deposition of F4-TCNQ, indicating the formation of unwanted electron–hole puddles due to an inhomogeneous doping profile [51,62]. These properties can be reflected in the on-current of the devices, thereby decreasing the on/off current ratio. Further investigations of dual molecular doping in combination with homogeneous and strong p-type and n-type dopants would be required for the development of highly functioning graphene FETs as digital electronic devices.

4. Graphene as a flexible transparent electrode material

4.1. Organic transistors based on graphene electrodes

Organic electronic devices using graphene electrodes have attracted considerable attention, and several reports have described the use of graphene source/drain electrodes in organic field-effect transistors (OFETs) [63–67]. An ultimate goal of the fabrication of OFETs using graphene electrodes lies in the fabrication of flexible transparent organic transistors, assembled on plastic substrates that maintain a high performance under ambient conditions. The use of graphene as an electrode material simultaneously requires several properties, including a high transmittance ($>90\%$), a low sheet resistance (10–$1000\ \Omega/sq$) and a work function that is amendable to ohmic contact with a semiconductor. Because the ratio of the intrinsic 2D DC conductivity to the optical conductivity (σ_{DC}/σ_{OP}) in graphene is limited, the optimization of the resistive properties without sacrificing the transmittance is fundamentally limited. In an effort to address this limitation, more interest has been focused on graphene doping because the tunable electrical properties of graphene are attainable via instantaneous doping [68–70]. Researchers have described the molecular doping of graphene using organic solvents, acids, salts, H_2O, ammonia, and several gas molecules. Park et al. introduced a sustainable, homogeneous n-type doping technique using the aligned dipole moments of amine-functionalized SAMs [66]. SAMs were introduced onto the SiO_2/Si substrate, and the doping profile could be easily patterned, as shown in
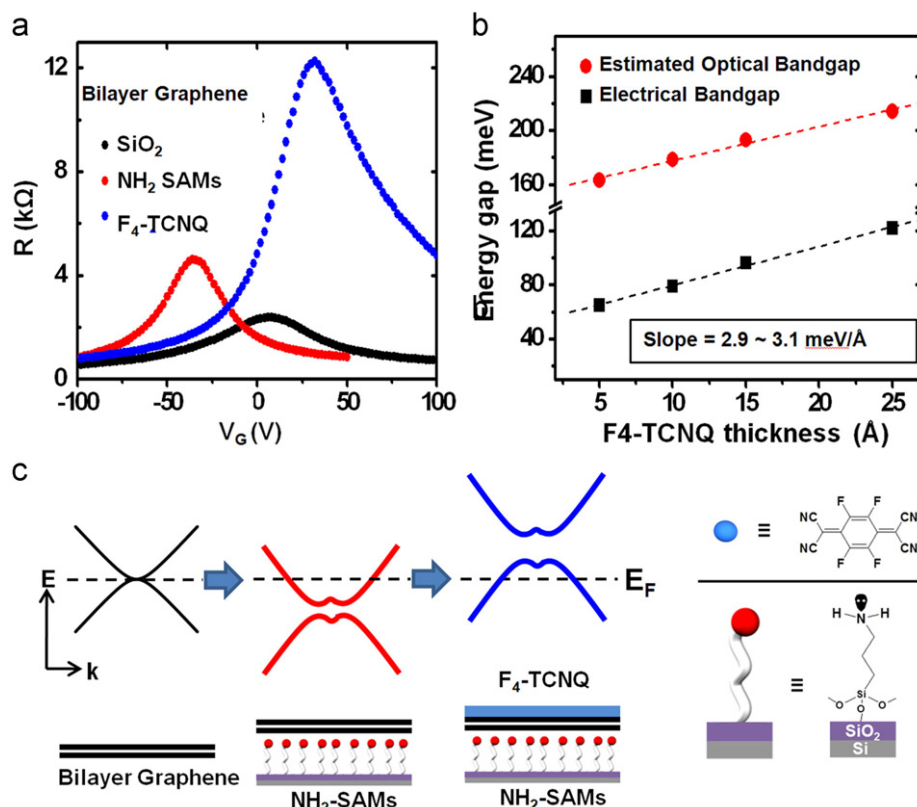
Fig. 4. (Color online) **Band gap-engineered bilayer graphene FETs**. (a) Current–voltage transfer characteristics of bilayer graphene FETs with molecular doping agents. SiO₂: untreated SiO₂/Si (no doping), NH₂: NH₂-SAM modified SiO₂/Si (n-doping), F₄-TCNQ: 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquino-dimethane (thickness of 10 Å, p-doping). (b) The plots for electrical bandgaps and estimated optical bandgaps as a function of F4-TCNQ thickness. (c) The electronic band structures of bilayer graphene on an untreated, NH₂-SAM modified SiO₂/Si substrate and F₄-TCNQ deposited bilayer graphene on a NH₂-SAM modified SiO₂/Si substrate (shown from left to right) (Reproduced from Ref. [60] with permission from Wiley).
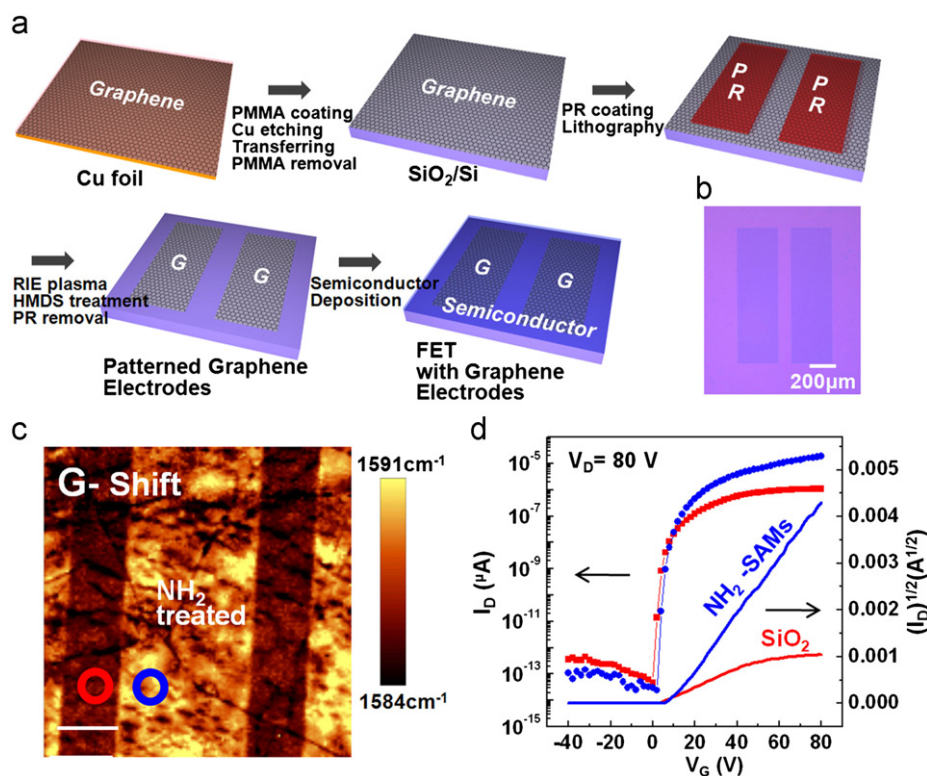

Fig. 5. (Color online) **Organic FETs based on monolayer graphene electrodes**. (a) Schematic of the fabrication of pentacene FETs with monolayer graphene electrodes on a SiO₂/Si substrate. (b) Optical microscopy image of patterned graphene electrodes. (c) Raman maps of G-band shift of monolayer graphene on SiO₂/Si substrate with patterned NH₂-SAMs. Scale bars are 10 μm (d) Transfer characteristics of PTCDI-C13 FETs with graphene S/D electrodes on different SAM-modified SiO₂. (Reproduced from Ref. [65] with permission from Wiley, Ref. [66] with permission from American Chemical Society).

Fig. 5(c). The resultant graphene work function shifted by 0.6 eV, which resulted in a 1 order of magnitude increase in the field effect mobility of the organic transistors based on a thin film n-type semiconductor, N, N-0-ditridecyl-3,4,9,10-perylenetetra-carboxylicdiimide (PTCDI-C13) (Fig. 5(d)).

A key issue blocking the use of graphene as an electrode is its mechanical stability and the feasibility of fabricating flexible OFETs. Fig. 5(a) shows a schematic diagram of the fabrication steps involved in patterning and transferring CVD-graphene to produce source/drain electrodes using a polymer-supported transfer method. Because graphene consists only of a planar honeycomb lattice one carbon atom thick, the film may be easily patterned by conventional photolithographic techniques, combined with reactive ion etching (RIE). CVD graphene can be patterned either before or after transfer to the target substrate. Lee et al. described the fabrication of organic transistors with a graphene electrode on plastic, focusing on the final development of the organic semiconductor morphology as a function of the fabrication process. A conventional transfer-pattern process was found to introduce severe damage into the channel region on the substrate during the dry etching process, which resulted in loosely packed small grains of organic semiconductors with a low interconnectivity; however, graphene patterning on the catalyst film (Cu) prior to the transfer process did not damage the substrate. Consequently, the field effect mobility increased by one order of magnitude. Monolayer graphene, with a high transparency and good conductivity, provides an alternative electrode material for use in next-generation flexible electronic devices assembled on plastic substrates.

4.2. 2D framework for inducing the oriented crystalline growth of organic semiconductor

The exceptionally high conductivity and transparency of intrinsic and doped graphene electrodes has been successfully employed in organic field-effect transistors (OFETs). The growth characteristics of organic semiconductors affected by the surface properties of graphene have received considerable attention, because the crystallographic size and organic semiconductor orientations determine the injection and transport of charge carriers [71,72]. Over the past several decades, the molecular arrangements of organic semiconductors on chemically driven graphene (reduced graphene oxide, rGO) or highly oriented pyrolytic graphite (HOPG) surfaces have been studied extensively [73–77]. Because most organic semiconductors consist of π-conjugated planar acenes, these molecules can interact with the underlying graphitic film surface via π–π interactions and are arranged according to a quasi-epitaxial growth mode. The molecular arrangement of perylene-3,4,9,10-tetracarboxylic dianhydride, a representative planar acene, on large-area epitaxial graphene grown on a SiC (0001) surface was recently studied by scanning tunneling microscopy (STM) [77].

Lee et al. recently reported the growth characteristics of pentacene, an organic semiconductor commonly used in OFETs, on CVD-grown monolayer graphene films [78]. The electrical properties were directly measured via the FET characteristics. During the transfer and patterning processes, impurities or polymer residues were inevitably physisorbed onto the graphene surfaces, which altered the chemical and physical properties of the graphene. Fig. 6(a) and (c) show 2D grazing angle incidence
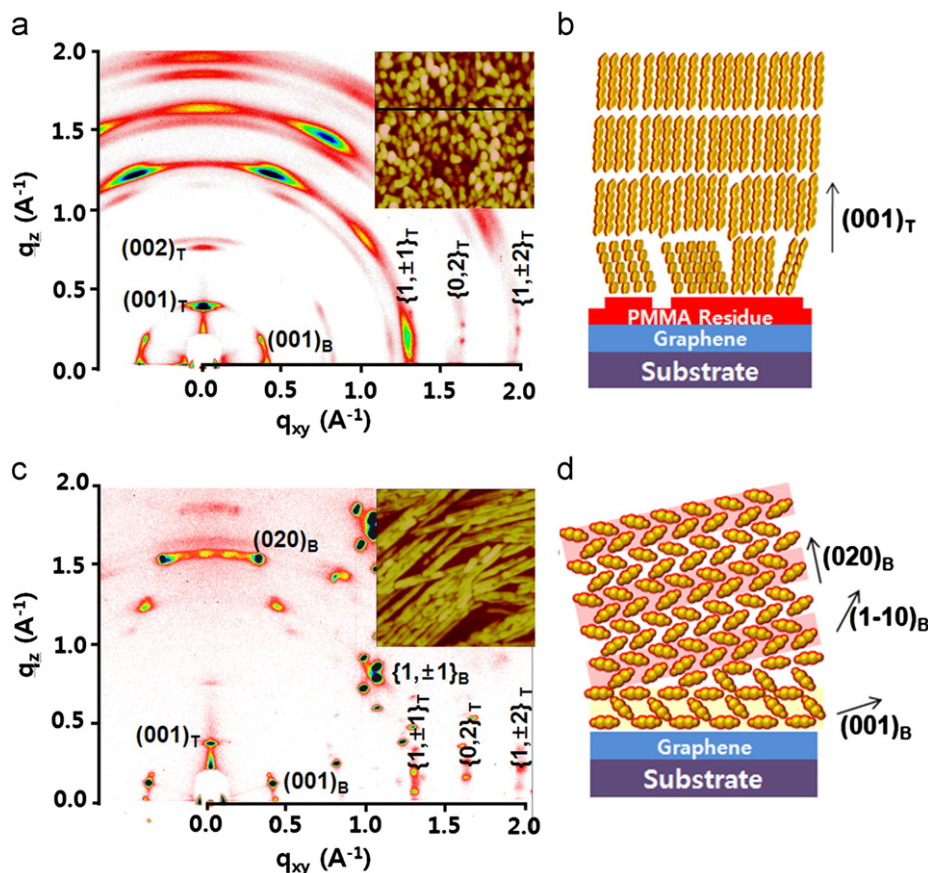

Fig. 6. (Color online) **Large area graphene as 2D framework for crystalline semiconductor growth.** 2D GIXD patterns of the 50 nm thick pentacene films deposited on (a) untreated graphene films and (c) thermally treated graphene films. The inset shows the AFM images collected during formation of the pentacene film on untreated graphene films. Schematic representations of the possible molecular packing orientations during growth of the pentacene film on (b) untreated graphene films and (d) thermally treated graphene films. (Reproduced from Ref. [78] with permission from American Chemical Society).

x-ray diffraction (2D GIXRD) images of a pentacene film (50 nm) grown on the as-prepared and thermally annealed graphene films. The crystallographic orientations of pentacene changed noticeably with the substrate conditions. The residual polymer (polymethylmethacrylate, PMMA) present on the graphene films after the transfer and photolithographic process prevented the graphene and pentacene from interacting, leading to an edge-on molecular arrangement of the pentacene, in which the (001) surface with the lowest surface energy was parallel to the substrate. The resultant OFET performance based on a graphene electrode with or without a PMMA residue clearly showed a distinctive performance. Because the pentacene growth in the hydrophobic channel region adopted an edge-on arrangement, the matched crystallographic orientations of the pentacene present between the graphene and channel regions decreased the contact resistance and, consequently, increased the field-effect mobility of the devices. Highly conductive graphene electrodes must be combined with the controlled molecular packing of organic semiconductors grown on graphene surfaces because this combination enhances the electrical properties of organic electronic devices based on graphene electrodes.

5. Conclusions and outlook

The large-area synthesis of graphene has undergone rapid development to yield high-quality, uniform 30 in. wafer-scale layers based on CVD processes. Large-area graphene to FETs or OFET devices has shown promise as a possible post-silicon material, a central step toward next-generation electronics, including soft electronics. From the use of chemical treatments to tune the intrinsic graphene properties to the use of molecular modulation on graphene for band gap engineering, graphene research has successfully enhanced the properties of graphene via several facile molecular doping methods. The application of graphene as a transparent flexible electrode material shows great potential for the realization of flexible electronics. The use of surface-modulated graphene as a 2D framework for semiconductor crystalline growth can provide new insights into the optimization of graphene electronics. With the development of new organic materials and device fabrication approaches, additional improvements in the performance of graphene-based transistors are possible toward the fabrication of high-performance transistor devices. In addition, the same approach will be utilized to enhance the performance of various large-area electronic and optical applications [80,81], including photovoltaic cells [82], light-emitting diodes [83–86], IR/THz devices [87–89], electro-thermal devices [90,91], plasmonic and laser applications [90–99].

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